WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a first wiring extending in a first direction;

a second wiring extending in a second direction differing from said first direction; and

a magneto resistive element arranged between said first wiring and said second wiring and comprising a first portion and a second portion, said second portion being in contact with said second wiring and extending along said second wiring to reach an outside region positioned outside said first portion.

2. The semiconductor memory device according to claim 1, wherein said second portion extends along said second wiring to reach at least an adjacent cell.

3. The semiconductor memory device according to claim 1, further comprising a constricted portion formed in the outside region, said constricted portion being formed in a portion where said second portion and said second wiring are narrower than said first portion.

4. The semiconductor memory device according to claim 1, further comprising a folded portion formed in the outside region, said folded portion being formed in a portion where said second portion and said second wiring are bent in a direction differing from said second direction.

5. The semiconductor memory device according to

claim 1, further comprising a transistor or a diode connected to said magneto resistive element.

6. The semiconductor memory device according to claim 5, wherein said diode is arranged between said magneto resistive element and said first wiring and is connected to said magneto resistive element and said first wiring.

7. The semiconductor memory device according to claim 1, wherein said magneto resistive element comprises:

a first magnetic layer;

a second magnetic layer; and

a first nonmagnetic layer interposed between said first magnetic layer and said second magnetic layer.

8. The semiconductor memory device according to claim 7, wherein said first portion comprises one of said first and second magnetic layers and said first nonmagnetic layer, and said second portion comprises the other of said first and second magnetic layers.

9. The semiconductor memory device according to claim 8, wherein a part of the other of said first and second magnetic layers is included in said first portion.

10. The semiconductor memory device according to claim 8, wherein said second portion is said second magnetic layer, and said second magnetic layer is a magnetic recording layer.

11. The semiconductor memory device according to claim 8, wherein said second portion is said first magnetic layer and said first magnetic layer is a magnetically fixed layer.

12. The semiconductor memory device according to claim 7, wherein said first portion is said first magnetic layer, and said second portion includes said first nonmagnetic layer and said second magnetic layer.

13. The semiconductor memory device according to claim 1, wherein said magneto resistive element comprises:

a first magnetic layer;

a second magnetic layer;

a third magnetic layer;

a first nonmagnetic layer sandwiched between said first and second magnetic layers; and

a second nonmagnetic layer sandwiched between said second and third magnetic layers.

14. The semiconductor memory device according to claim 13, wherein said first portion includes one of said first and third magnetic layers and said first and second nonmagnetic layers, and said second portion includes the other of said first and third magnetic layers.

15. The semiconductor memory device according to claim 14, wherein a part of the other of said first and third magnetic layers is included in said first

portion.

16. The semiconductor memory device according to claim 14, wherein said first and third magnetic layers are magnetically fixed layers.

17. A method of manufacturing a semiconductor memory device provided with a magneto resistive element including a first portion and a second portion, comprising:

extending said second portion along a second wiring to reach an outside region positioned outside said first portion by patterning said second portion together with said second wiring.

18. The method of manufacturing a semiconductor memory device according to claim 17, further comprising, before patterning said second portion together with said second wiring:

forming a first wiring;

forming said first portion above said first wiring; and

forming said second portion and said second wiring on said first portion.

19. The method of manufacturing a semiconductor memory device according to claim 17, further comprising, after patterning said second portion together with said second wiring:

forming said first portion on said second portion; and

forming a first wiring above said first portion.

20. The method of manufacturing a semiconductor memory device according to claim 17, further comprising forming a constricted portion in the outside region, said constricted portion being positioned in a region where said second portion and said second wiring are rendered narrower than said first portion.

21. The method of manufacturing a semiconductor memory device according to claim 17, further comprising forming a folded portion in the outside region, said folded portion being a portion where said second portion and said second wiring are bent in a direction differing from a direction in which said second wiring extends.

22. The method of manufacturing a semiconductor memory device according to claim 17, wherein said second portion extends along said second wiring to reach at least an adjacent cell.

23. The method of manufacturing a semiconductor memory device according to claim 17, wherein said magneto resistive element comprises:

a first magnetic layer;

a second magnetic layer; and

a first nonmagnetic layer sandwiched between said first and second magnetic layers.

24. The method of manufacturing a semiconductor memory device according to claim 23, wherein said first

portion includes said first magnetic layer and said first nonmagnetic layer, and said second portion includes said second magnetic layer.

25. The method of manufacturing a semiconductor memory device according to claim 24, wherein a part of said second magnetic layer is included in said first portion.

26. The method of manufacturing a semiconductor memory device according to claim 23, wherein said first portion includes said first magnetic layer, and said second portion includes said first nonmagnetic layer and said second magnetic layer.

27. The method of manufacturing a semiconductor memory device according to claim 17, wherein said magneto resistive element comprises:

a first magnetic layer;

a second magnetic layer;

a third magnetic layer;

a first nonmagnetic layer sandwiched between said first and second magnetic layers; and

a second nonmagnetic layer sandwiched between said second and third magnetic layers.

28. The method of manufacturing a semiconductor memory device according to claim 27, wherein said first portion includes the first magnetic layer, the second magnetic layer, the first nonmagnetic layer and the second nonmagnetic layer, and said second portion

includes a third magnetic layer.

29. The method of manufacturing a semiconductor memory device according to claim 28, wherein a part of said third magnetic layer is included in said first portion.